UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,107	03/15/2004	Takayoshi Obinata	81754.0110	9251

26021 7590 03/07/2006

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/801,107	OBINATA, TAKAYOSHI	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *18-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 18-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12-22-5.

Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-17 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Nakajo (20020127776).

In the abstract, and paragraphs 20, 24, 29, 76-81, 102, 158-179, 181-188 and claim 1, Nakajo discloses the following:

A semiconductor device 20J, comprising: a semiconductor chip 22 including an integrated "circuit"; an interconnect 25 inherently electrically connected to the integrated circuit; a pad 25 that is a part of the interconnect and disposed on a front surface of the semiconductor chip; wirings 26 electrically connected to the pad; an external terminal 23 provided over and electrically connected to the wirings; and a resin layer 40 surrounding the external terminal and extending to a side face of the semiconductor chip; wherein the semiconductor chip has a thin-wall part at edges thereof, and the resin layer extends to the thin-wall part; wherein the semiconductor chip has a first face perpendicularly descending from the front surface, a second face perpendicularly ascending from a back surface opposite to the front surface, and a third face 50 parallel (illustrated in FIG. 29 (E)) to the front surface and connecting the first face with the second face, and the resin layer formed on the first face, but not on the second face; wherein the semiconductor chip has a first face 53 perpendicularly (at least very steeply) descending from the front surface, a second face perpendicularly ascending from a back surface opposite to the front surface, and a third face 43, 50 that curves (illustrated in FIGS. 27(B), 27(C) and 27(D)) to connect the first face with the second face, and the resin layer is formed on the first face, but not on the second face; wherein the resin layer is also formed on the third face; wherein the semiconductor chip comprises a

first face 53 descending from the front surface and a second face ascending from a back surface opposite to the front surface, the first face and the second face being formed at different angles, and the resin layer formed on the first face, but not on the second face; wherein the semiconductor chip comprises a first face 53 curved in a descending manner from the front surface and a second face vertically ascending from a back surface opposite to the front surface, and the resin layer formed on the first face, but not on the second face; an inherent stress relaxation layer 28 formed on the semiconductor chip, wherein the wirings are formed on the stress relaxation layer and the resin layer is formed over the stress relaxation layer; an inherent resist layer 28 covering the wirings other than a region for providing the external terminal, wherein the resin layer is formed over the resist layer.

A circuit "board" on which a semiconductor device according to claim 1 is mounted.

An electronic apparatus 20J comprising a semiconductor device according to claim 1.

A semiconductor wafer, comprising: a semiconductor substrate 35 including a plurality of integrated circuits; an interconnect electrically connected to each of the integrated circuits; pads that are parts of the interconnect and disposed on a front surface of the semiconductor substrate,

wherein grooves 52 are formed in the front surface; wirings electrically connected to the pads; external terminals provided over and electrically connected to the wirings; and a resin layer surrounding the external terminals and covering the grooves; wherein the grooves inherently surround each of the integrated circuits; wherein a side face and a bottom face of each groove are connected via a curved surface; wherein a face of each groove is inclined; a stress relaxation layer formed on the semiconductor substrate, wherein the wirings are formed on the stress relaxation layer and the resin layer is formed over the stress relaxation layer; a resist layer covering the wirings other than a region for providing the external terminals, wherein the resin layer is formed over the resist layer.

To further clarify the disclosure of an inherent stress relaxation layer 28, the language "stress relaxation" is a statement of intended use of the layer that does not appear to result in a structural difference between the claimed layer and the layer of Nakajo. Further, because the layer of Nakajo appears to have the same structure as the claimed layer, it appears to be inherently capable of being used for the intended use, and the statement of intended use does not patentably distinguish the claimed layer from the layer of Nakajo. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546,

1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Indeed, Nakajo discloses that layer 28 is polyimide, and in the specification, paragraph 39, applicant discloses that a polyimide layer is a stress relaxation layer.

Also, Nakajo discloses an inherent resist layer 28 because layer 28 is a coating that inherently protects against a chemical, electrical, or physical action. Indeed, as cited, Nakajo discloses, "film protecting the circuit surface, generally a polyimide film." In any case, the term "resist" merely limits the scope of the layer of Nakajo to the intended use of the layer and

does not appear to result in a structural difference between the claimed layer and the layer of the applied prior art. Further, because the layer of Nakajo appears to have the same structure as the claimed layer, it appears to be inherently capable of being used for the intended use, and the intended use does not patentably distinguish the claimed layer from the layer of Nakajo. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajo (20020127776).

It is not apparent if Nakajo explicitly discloses the applied embodiments of FIGS. 25-27, 29 and 30 in combination with the other applied embodiments.

In any case, it would have been obvious to combine the applied embodiments of FIGS. 25-27, 29 and 30 with the other applied embodiments because, as disclosed by Nakajo as cited, it would improve device reliability and reduce manufacturing cost of the other applied embodiments.

Claim 13 is alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajo as applied to claim 13 supra, and further in combination with Hutson (3608186).

Hutson does not appear to explicitly disclose that the grooves surround each of the integrated circuits.

Nevertheless, at column 4, lines 26-39; and column 4, line 74 to column 5, line 12, Hutson discloses wherein "grooves" surround integrated circuits "devices." Moreover, it would have been obvious to combine this disclosure of Hutson with the disclosure of Nakajo because it would facilitate the cutting "into the respective semiconductor devices" of Nakajo.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
2-Mar-06